A 2 GHZ PULSE COUNTER

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Abstract

A counter able to process pulses of random distribution with repetition rates up to 2 GHz employs tunnel diodes in the input circuit and in the fastest flipflops. The outer circuits contain ECL and TTL ICs. Function and theory are discussed.

Introduction

For development as well as for performance tests of Gigabit Data-Rate Systems, measurement of the error rate - which is one of the main system parameters - becomes difficult, because a counter is required capable to count pulses of random distribution with a maximum rate in the gigahertz range.

This paper describes a random pulse counter for 2 GHz max. counting rate which could very well serve as an error rate measuring equipment for ultra high speed data transmission.

General Considerations

Constructing a fast random pulse counter one has primarily to solve the problems of wide band fast rise input circuits (gate, instantaneous limiter, threshold circuit, pulse shaper) besides providing a flipflop fast enough for the least significant bit.

With transistors of today's technical standard it is difficult to realize circuits capable to process data at rates beyond 1 GHz. Tunnel diodes switching fast enough for that purpose are easily available and therefore were chosen for the fast circuits.

The block diagram (Fig. 1) gives an idea of the components of the counter and their interconnections.

Input Circuits

As shown in Fig. 2, the counter contains a 3 stage tunnel diode input circuit acting as a limiter, discriminator, and pulse shaper, which allows the direct application of 1 Vpp signals without preamplifier. Thus, ECL signals can be used as a source, requiring only a bias shifter.

By superposing a rectangular pulse to the bias of one of the input stages, very fast gating action can be obtained. The fast rise gating pulse may be provided by an high-speed emitter coupled transistor circuit or - even faster - using step recovery diodes.

For error rate measurements, however, which are generally made during long time intervals, a fast gate will not be necessary. In that case it is sufficient to use standard circuits for gating pulse generation.

By the third input stage the random signal is converted to a series of pulses properly shaped to trigger the first flipflop, with the same random distribution as that of the original signal except for the limitation of minimum distance to about 0.5 ns.

Counting Flipflops

The first three flipflops contain tunnel diodes as active elements. The logical function is that of T-flipflop type. Several circuits that realize this function using tunnel diode pairs as bistable elements and reactances or delay lines as a dynamic memory have been published. All of them are suitable for gigahertz data rates and have been tested successfully.

The circuit presently used employs inductors for dynamic memory action. It was chosen mainly due to technological reasons (taking profit of stray inductance) and may be allotted to the same class of circuits as those described in the references.[1,2]

Flipflop Interconnection

To achieve maximum counting rate, a code must be chosen which requires no feedback in order to avoid delay.

This leads to the use of straight binary code which permits simple cascading of the flipflops. The lacking isolation of the tunnel diode flipflops can be sufficiently replaced by inserting monostable tunneldiode circuits which additionally provide pulse regeneration.

Counting of random signals requires differentiation of each flipflop output pulse. On the other hand, the flipflops must be terminated by a nearly frequency independent load. This can be achieved by upgrading the differentiator pad to a complete branching filter. The upper band output feeds the adjoining stage, the lower band output (static output) is used for display. This allows a very economic use of flipflop output power. The output of the third counting stage is connected to the base of a single transistor which shifts the level to ECL standard level.

Counting Code

Binary

As mentioned above, straight binary code is indicated for the fastest stages and actually the simplest 2-GHz-counter is obtained by adding the necessary number of flipflops in cascade connection. Such a binary counter which will be suitable for most

ways of data processing has been constructed and worked satisfactorily. This is also the type the block diagram refers to.

Decimal

For optical readout decimal code is desired. In order to avoid loss of speed, binary counting by the fastest three flip-flops shall be maintained. The methods for conversion into decimal code known so far are rather complicated and expensive.[3,4]

In the present case, these difficulties have been overcome by means of a rather simple computing device which is made of standard integrated ECL components. It consists of a 3-flipflop multiply-with-8 circuit which has a one decimal digit product output and a carry output, a two bit binary full adder and binary subtracting device. The product output and the data stored in the three tunnel diode flipflops are added and the sum will be reduced by 10 if the multiplier carry is "one". The computing circuit is completed by a few NOR gates and provides a correct decimal reading if the carry output of the multiplier is connected to a conventional BCD counter.

Technology

All the gigahertz tunnel diode stages (input and flipflop circuits) are realized in thin and thick film hybrid technology. Striplines and other leads are etched or screen-printed respectively, resistors, capacitors, and inductors are screen-printed only. The substrates used are of alumina ceramics, the size being 1 inch x 1 inch for the input filter, 1 inch x 0.5 inch for the 3-stage input circuit, and 1 inch x 0.4 inch for each flipflop. The tunnel diodes (micropill package) are bonded to the substrates by soldering. Fig. 3 shows the array of the hybrid circuits.

Performance, Reliability

The circuit is designed to operate over a temperature range from 0 to +55 degrees centigrade within a power supply voltage range from 10 to 17 volts.

The gigahertz circuits were operated for 500 hours at 115 degrees centigrade without any measurable degradation of tunnel diode parameters (manufacturer: Siemens).

The counter showed excellent operation within a frequency range from 0 to the upper limit when the following waveforms were applied: sinewave, triangular and rectangular waves in the range of < 1 Hz up to above 2 GHz (upper limit sinewave only), as well as single spikes, trains, and bursts of spikes with pulse distances continuously varied down to less than 0.5 ns.

The oscillogram of Fig. 4 demonstrates the response to a sinewave signal of 2110 MHz. Fig. 5 is a photograph of the complete high speed part of the counter.

Theory

Fig. 6 shows a universal equivalent circuit that can be used for computer simulation of all the known tunnel diode pair gigahertz flipflops. The adaptation of the model to the properties of the circuit under test simply is performed by allotting a special set of constants to the parameters of the generalized equivalent circuit. For calculation the tunnel diodes are represented by analytic nonlinear expressions for their resistive I-V characteristic combined with linear capacitances and inductances. The other components of the circuit are linear, too.

The circuit behavior is described by the differential equations of the network. These equations are numerically integrated by means of a digital computer to obtain the signal waveforms in the time domain. The good congruence of calculated and measured waveforms is demonstrated by Fig. 7. The differential equations are also the base for a stability analysis.

Conclusion

A reliable 2 GHz random pulse counter has been realized that might be useful for measurements in gigabit data rate systems as well as for many other applications, e.g. digital frequency control and programming of microwave oscillators, time interval, and short range distance measurements, and nuclear research.

Acknowledgements

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References

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2. H.G. Jungmeister: Eine bistabile Kippstufe für den Gigahertzbereich, Arch. Elektr. Übertrag. 21(1967), p 447 - 458

3. DBP 873910

4. Operator's Manual of the 210 MHz counter manufactured by Takeda Riken Japan

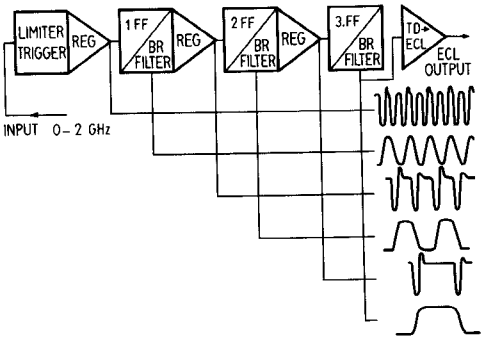

Fig. 1: Block Diagram of a 2 GHz Counter

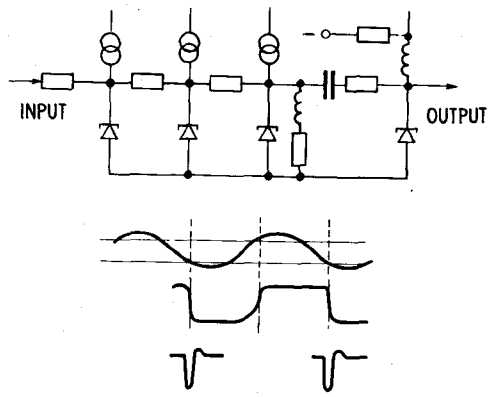

Fig. 2: Input Circuit

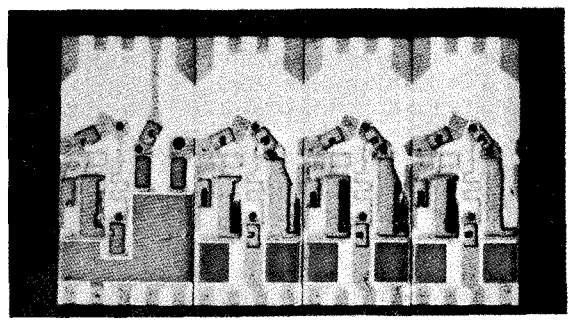

Fig. 3: Array of Thick Film Circuits
(input circuit and 3 flipflops)

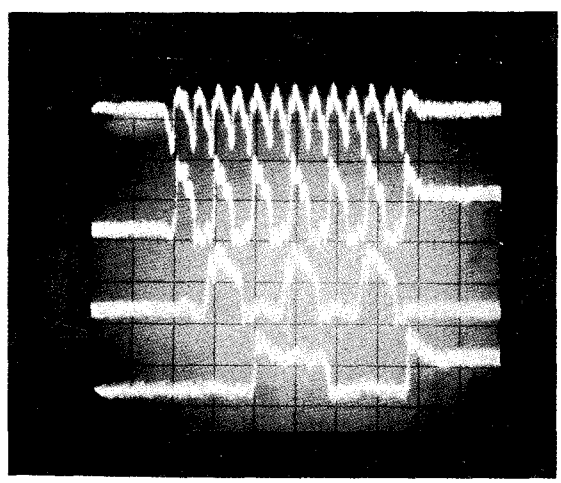

Fig. 4: Counter Waveforms
Upper trace: pulses shaped by the input circuit. Input: gated sine-wave of 2110 MHz.
3 lower traces: flipflop outputs;
Horizontal scale: 1 ns/div

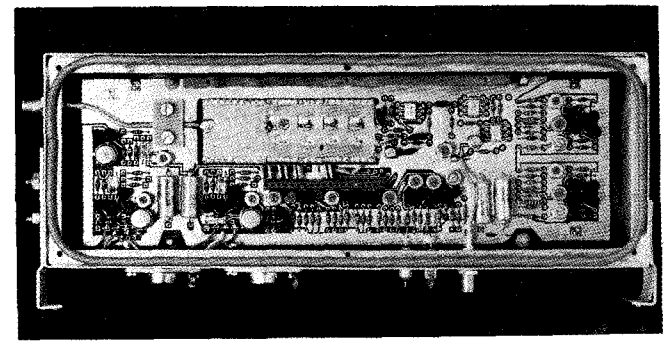

Fig. 5: View of High Speed Part of the Counter

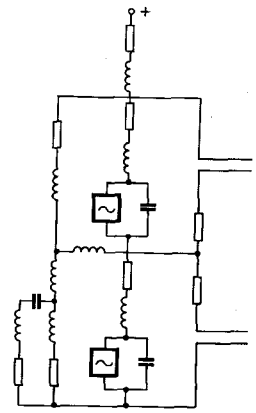

Fig. 6: Generalized Equivalent Circuit of Tunnel Diode Pair Flipflops

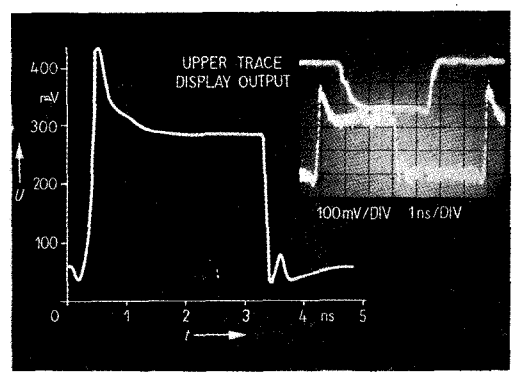

Fig. 7: Comparison of Calculated and Measured Waveforms